AMENTMENTS

In The Claims:

1. (currently amended) A chip package structure comprising:

at least an integrated circuit die;

a metal layer deposited over said integrated circuit die and extending to a place under which there is no integrated circuit die; and

at least a passive device electrically connected to said integrated circuit die.

~~an organic substrate;~~

~~a die, wherein the die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of the die is adhered to the organic substrate; and~~

~~a thin-film circuit layer located on top of the organic substrate and the die and has an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to the corresponding metal pad of the die.~~

Claims 2-5 (canceled)

6. (currently amended) The structure in claim 1 further comprising a substrate under said integrated circuit die. ~~, wherein the thin-film circuit layer comprising at least a patterned wiring layer and a dielectric layer, the dielectric layer is located on top of the organic substrate and the~~

~~die, and the patterned wiring layer is located on top of the dielectric layer, whereas the patterned wiring layer is electrically connected to the metal pads of the die through the dielectric layer and forms the external circuitry and the bonding pads of the external circuitry.~~

7. (currently amended) The structure in claim 1~~-6~~ further comprising a dielectric layer over said integrated circuit die, said metal layer deposited on said dielectric layer and electrically connected to said integrated circuit die through at least a via in said dielectric layer. ~~, wherein the dielectric layer has a plurality of thru-holes, and the patterned wiring layer is electrically connected to the metal pads of the die by the thru-holes.~~

8. (currently amended) The structure in claim 1~~-6~~ further comprising a dielectric layer on said metal layer. ~~, wherein a via is located inside each thru-hole, and the patterned wiring layer is electrically connected to the metal pads of the die by the vias.~~

9. (currently amended) The structure in claim 1~~-6~~ further comprising a plurality of said integrated circuit dies, said metal layer electrically connecting said integrated circuit dies. ~~, wherein the patterned wiring layer and the vias form the external circuitry.~~

Claims 10-12 (canceled)

13. (currently amended) The structure in claim 1~~-6,~~ further comprising a film layer around said integrated circuit die, and said metal layer further extending over said film layer. ~~wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.~~

14. (currently amended) The structure in claim 13~~-1~~ further comprising a substrate under said integrated circuit die and under said film layer. ~~, wherein the thin film circuit layer~~

~~comprising a plurality of patterned wiring layers and a plurality of dielectric layers, in which the patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is formed between the thin film circuit layer and the organic substrate, the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die through the dielectric layer that is closest to the organic substrate, where the patterned wiring layer that is furthest away from the organic substrate forms the bonding pads.~~

15. (currently amended) The structure in claim 13~~-14~~, wherein said film layer has a surface coplanar with an active surface of said integrated circuit die. ~~each of the dielectric layers has a plurality of thru holes, by which each of the patterned wiring layer is electrically connected the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die through the dielectric layer.~~

16. (currently amended) The structure in claim 1~~-15,~~ further comprising a substrate, wherein said substrate has at least a cavity accommodating said integrated circuit die, said substrate having a surface coplanar with an active surface of said integrated circuit die, and said metal layer further extending over said surface of said substrate. ~~wherein a via is located in each thru hole, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die by the vias.~~

17. (currently amended) The structure in claim 1 ~~16~~, wherein said integrated circuit die has an active surface, said metal layer deposited over said active surface of said integrated circuit die. ~~the patterned wiring layers and the vias form the external circuitry.~~

Claims 18-24 (canceled)

25. (currently amended) The structure in claim 1, wherein said passive device comprises a resistor. ~~further comprising a filling layer located between a surface of the organic substrate and the thin film circuit layer and surrounding the peripheral of the die, and a surface of the filling layer is planar to the active surface of the die.~~

26. (currently amended) The structure in claim 1 ~~25~~, wherein said passive device comprises a capacitor. ~~a material of the filling layer is selected from a group consisting of epoxy and polymer.~~

27. (currently amended) The structure in claim 1, wherein said passive device comprises an inductor. ~~further comprising a passivation layer located on top of the thin film circuit layer and exposing the bonding pads.~~

28. (currently amended) The structure in claim 1 further comprising at least a bump deposited over said integrated circuit die or at a place under which there is no integrated circuit die, wherein said bump comprises solder. ~~a plurality of bonding points located on the bonding pads.~~

29. (currently amended) The structure in claim 1 ~~28~~ further comprising at least a bump deposited over said integrated circuit die or at a place under which there is no integrated circuit

die, wherein said bump comprises gold. ~~, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.~~

Claims 30-175 (canceled)

176. (currently amended) A chip package structure comprising:

at least an integrated circuit die;

a metal layer deposited over said integrated circuit die and extending to a place under which there is no integrated circuit die; and

at least a passive device deposited at a place under which there is no integrated circuit die.

~~an organic substrate;~~

~~a die module comprising an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of the die module is adhered to the organic substrate;~~

~~a filling layer located on top of the organic substrate and surrounding a peripheral of the die module, a top surface of the filling layer is planar to the active surface of the die module;~~

~~a thin organic layer located on top of the filling layer and the die module; and~~

~~a thin film circuit layer located on top of the thin organic layer and the die module and has an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die module and extends to a region outside the active surface of the die module, the external circuitry has a plurality of bonding pads located on a surface layer of the thin film circuit~~

~~layer and each bonding pad is electrically connected to a corresponding metal pad of the die module.~~

177. (currently amended) The structure in claim 176 further comprising a plurality of said integrated circuit dies, said metal layer electrically connecting said integrated circuit dies. ~~, wherein the die module comprising a single die.~~

Claims 178-179 (canceled)

180. (currently amended) The structure in claim 176 further comprising a substrate under said integrated circuit die. ~~, wherein a material of the filling layer is selected from a group consisting epoxy and polymer.~~

Claims 181-185 (canceled)

186. (currently amended) The structure in claim 176 further comprising a dielectric layer over said integrated circuit die, said metal layer deposited on said dielectric layer and electrically connected to said integrated circuit die through at least a via in said dielectric layer. ~~, wherein the thin film circuit layer comprising at least a patterned wiring layer, which is located on the thin organic layer, whereas the patterned wiring layer is electrically connected to the metal pads of the die module through the thin organic layer and forms the external circuitry and the bonding pads of the external circuitry.~~

187. (currently amended) The structure in claim 176 ~~186~~, wherein said passive device comprises a capacitor. ~~the thin organic layer has a plurality of thru holes, and the patterned wiring layer is electrically connected to the metal pads of the die module by the thru holes.~~

188. (currently amended) The structure in claim 176~~-187~~ further comprising a dielectric layer on said metal layer. ~~wherein a via is located inside each thru hole, and the patterned wiring layer is electrically connected to the metal pads of the die module by the vias.~~

189. (currently amended) The structure in claim 176~~-188~~, wherein said integrated circuit die has an active surface, said metal layer deposited over said active surface of said integrated circuit die. ~~the patterned wiring layer and the vias form the external circuitry.~~

Claims 190-192 (canceled)

193. (currently amended) The structure in claim 176 further comprising a film layer around said integrated circuit die, said metal layer further extending over said film layer, and said passive device deposited over said film layer. ~~, wherein the thin film circuit layer comprising a plurality of patterned wiring layers and a plurality of dielectric layers, in which the patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is formed between the thin film circuit layer and the organic substrate, the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die module through the dielectric layer that is closest to the organic substrate, where the patterned wiring layer that is furthest away from the organic substrate forms the bonding pads.~~

194. (currently amended) The structure in claim 193 further comprising a substrate under said integrated circuit die and under said film layer. ~~, wherein the thin organic layer has a plurality of first thru holes, by which the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die module, and each dielectric layer~~

~~has a plurality of second thru-holes, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring layers.~~

195. (currently amended) The structure in claim 193~~-194~~, wherein said film layer has a surface coplanar with an active surface of said integrated circuit die. ~~a first via is located inside each first thru-hole and a second via is located inside each second thru-hole, and each patterned wiring layer is electrically connected to the neighboring patterned wiring layers by the second vias, wherein the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die module by the first vias.~~

196. (currently amended) The structure in claim 176 further comprising a substrate, wherein said substrate has at least a cavity accommodating said integrated circuit die, said substrate having a surface coplanar with an active surface of said integrated circuit die, said metal layer further extending over said surface of said substrate, and said passive device deposited over said surface of said substrate. ~~195, wherein the patterned wiring layers, the first vias, and the second vias form the external circuitry.~~

Claims 197-199 (canceled)

200. (currently amended) The structure in claim 176~~-193,~~ further comprising at least a bump deposited over said integrated circuit die or at a place under which there is no integrated circuit die, wherein said bump comprises solder. ~~wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.~~

Claim 201. (canceled)

202. (currently amended) The structure in claim 176 further comprising at least a bump deposited over said integrated circuit die or at a place under which there is no integrated circuit die, wherein said bump comprises gold. ~~a plurality of bonding points located on the bonding pads.~~

203. (currently amended) The structure in claim 176~~-202~~, wherein said passive device comprises a resistor. ~~the bonding points are selected from a group consisting of solder balls, bumps, and pins.~~

204. (new) The structure in claim 1, wherein said passive device comprises a wave guide.

205. (new) The structure in claim 1, wherein said passive device comprises a filter.

206. (new) The structure in claim 1, wherein said passive device comprises a micro electronic mechanical sensor (MEMS).

207. (new) The structure in claim 1, wherein said passive device deposited over said integrated circuit die.

208. (new) The structure in claim 1, wherein said passive device deposited at a place under which there is no integrated circuit die.

209. (new) The structure in claim 176, wherein said passive device comprises an inductor.

210. (new) The structure in claim 176, wherein said passive device comprises a wave guide.

211. (new) The structure in claim 176, wherein said passive device comprises a filter.

212. (new) The structure in claim 176, wherein said passive device comprises a micro electronic mechanical sensor (MEMS).

213. (new) A chip package structure comprising:

at least an integrated circuit die;

a metal layer deposited over said integrated circuit die and extending to a place under which there is no integrated circuit die; and

at least a passive device deposited over said integrated circuit die.

214. (new) The structure in claim 213 further comprising a plurality of said integrated circuit dies, said metal layer deposited over said integrated circuit dies.

215. (new) The structure in claim 213 further comprising a substrate under said integrated circuit die.

216. (new) The structure in claim 213 further comprising a dielectric layer over said integrated circuit die, said metal layer deposited on said dielectric layer and electrically connected to said integrated circuit die through at least a via in said dielectric layer.

217. (new) The structure in claim 213 further comprising a dielectric layer on said metal layer.

218. (new) The structure in claim 213, wherein said integrated circuit die has an active surface, said metal layer deposited over said active surface of said integrated circuit die.

219. (new) The structure in claim 213 further comprising a film layer around said integrated circuit die, said metal layer further extending over said film layer.

220. (new) The structure in claim 219 further comprising a substrate under said integrated circuit die and under said film layer.

221. (new) The structure in claim 219, wherein said film layer has a surface coplanar with an active surface of said integrated circuit die.

222. (new) The structure in claim 213 further comprising a substrate, wherein said substrate has at least a cavity accommodating said integrated circuit die, said substrate having a surface coplanar with an active surface of said integrated circuit die, said metal layer further extending over said surface of said substrate.

223. (new) The structure in claim 213 further comprising at least a bump deposited over said integrated circuit die or at a place under which there is no integrated circuit die, wherein said bump comprises solder.

224. (new) The structure in claim 213 further comprising at least a bump deposited over said integrated circuit die or at a place under which there is no integrated circuit die, wherein said bump comprises gold.

225. (new) The structure in claim 213, wherein said passive device comprises a resistor.

226. (new) The structure in claim 213, wherein said passive device comprises a capacitor.

227. (new) The structure in claim 213, wherein said passive device comprises an inductor.

228. (new) The structure in claim 213, wherein said passive device comprises a wave guide.

229. (new) The structure in claim 213, wherein said passive device comprises a filter.

230. (new) The structure in claim 213, wherein said passive device comprises a micro electronic mechanical sensor (MEMS).